

# Beryll

Module Name	Rev.	Date of Issue	Document Number
Beryll	A	2014.2.20	S12-007

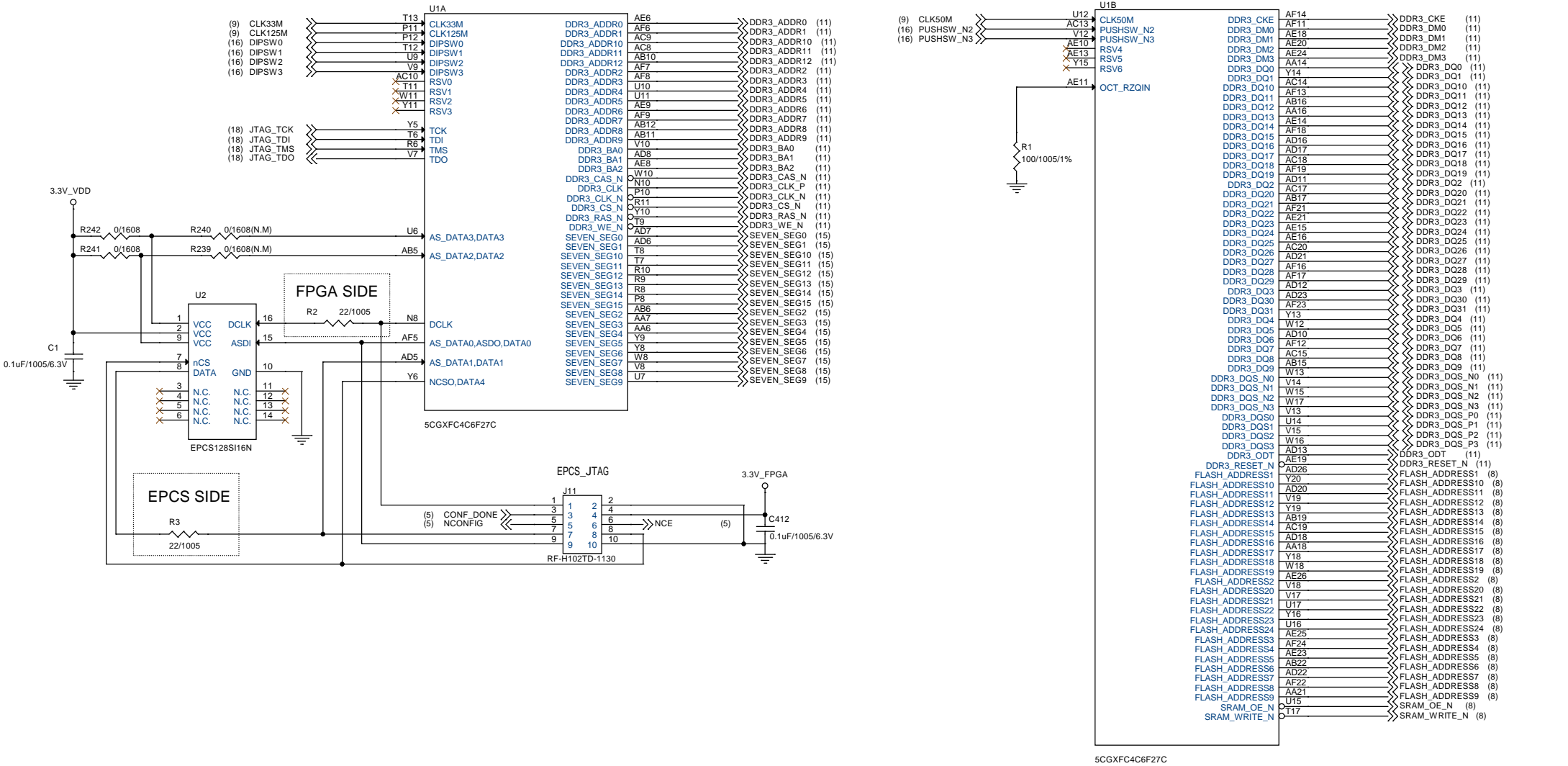
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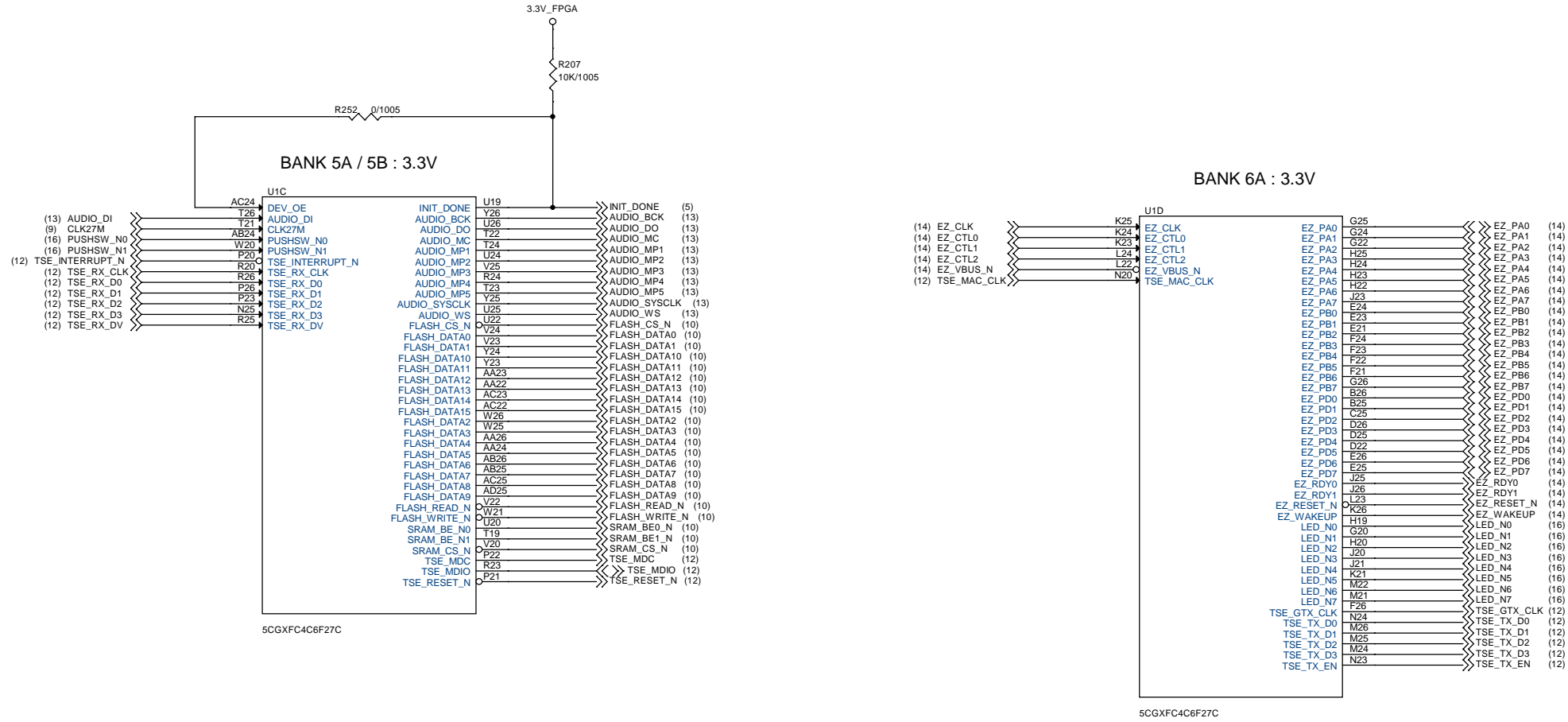
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BANK 3A : 2.5V, BANK 3B : 1.5V

BANK 4A : 1.5V

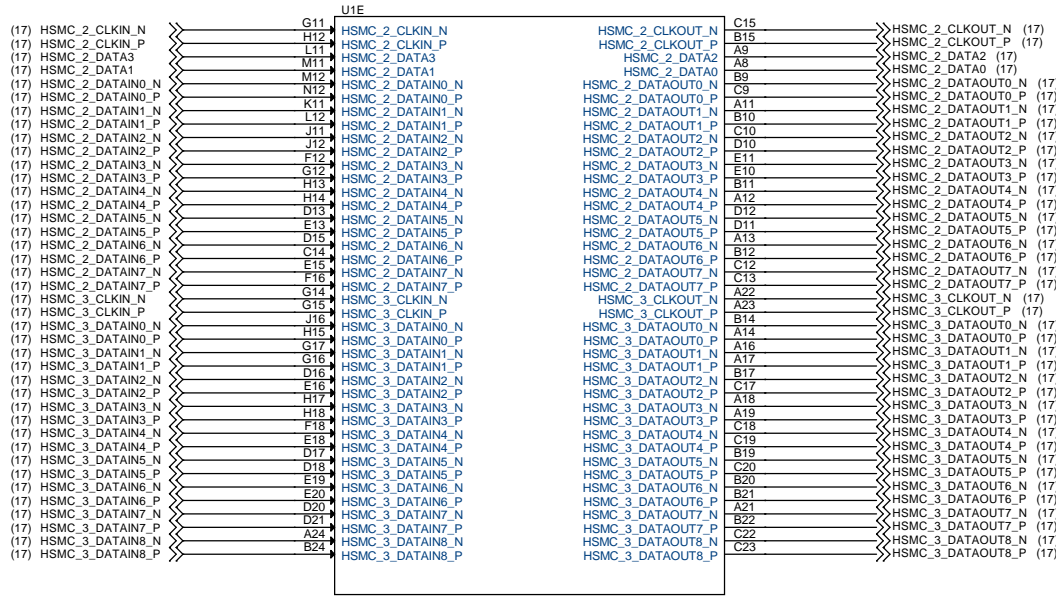


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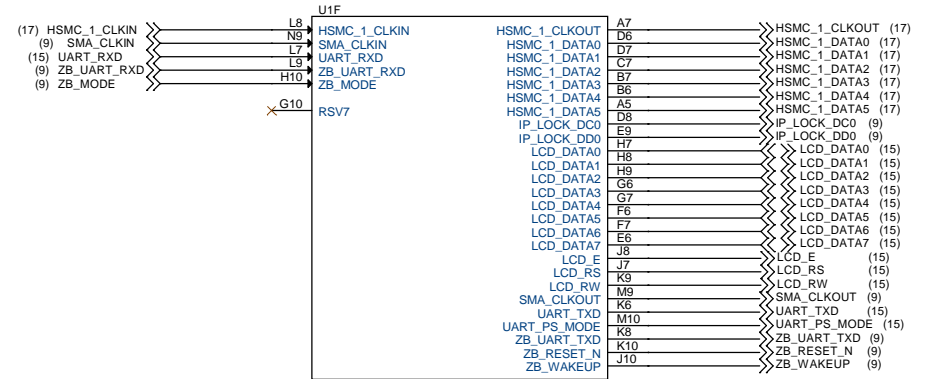
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BANK 7A : 2.5V

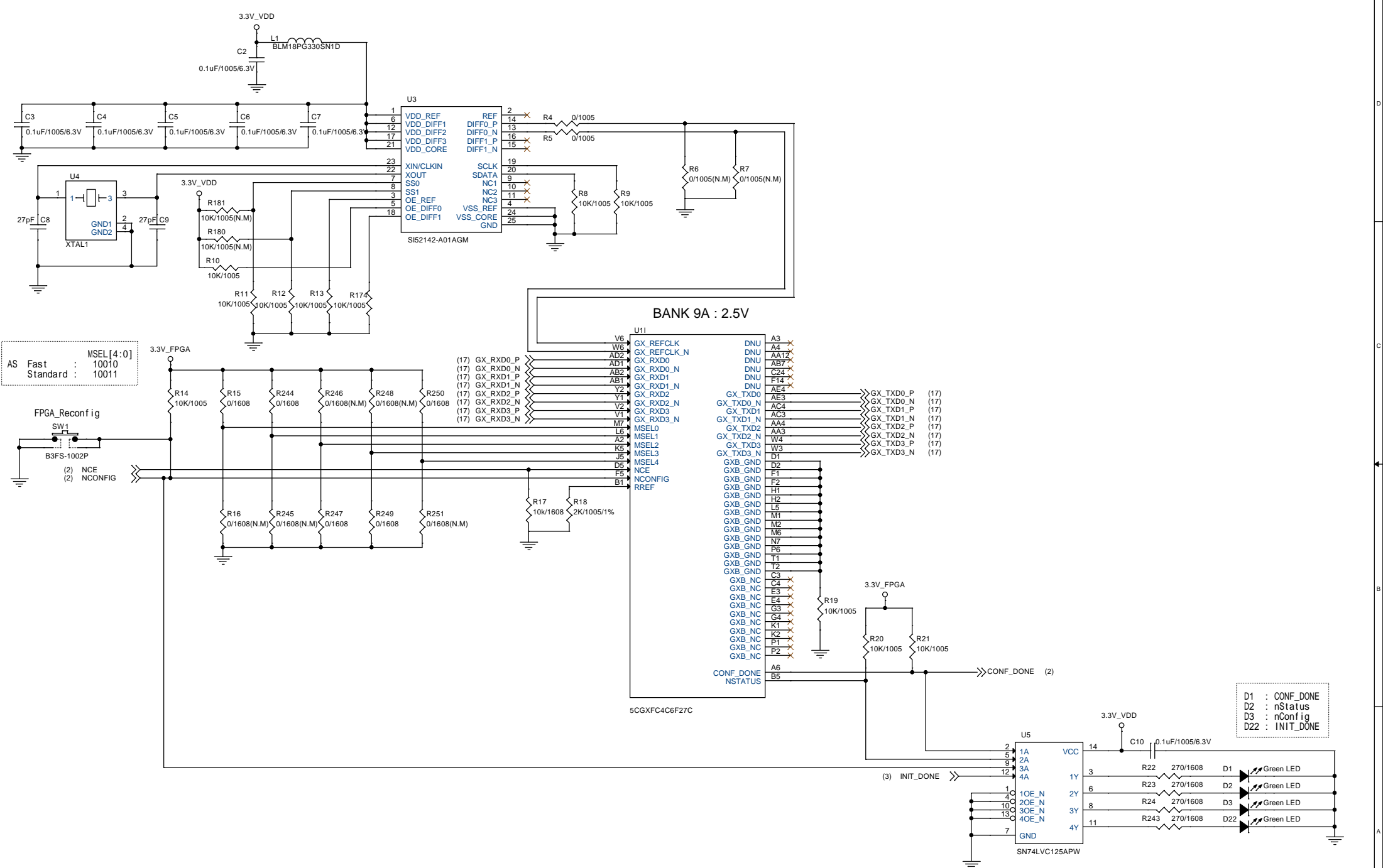


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BANK 8A : 2.5V



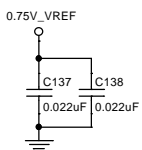
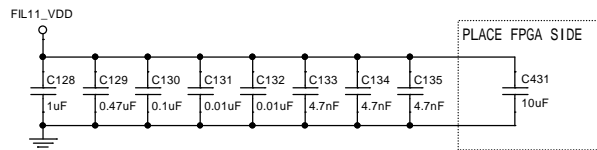
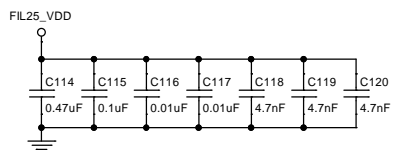
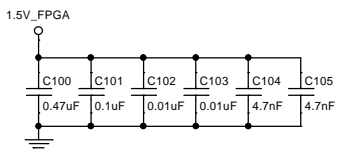
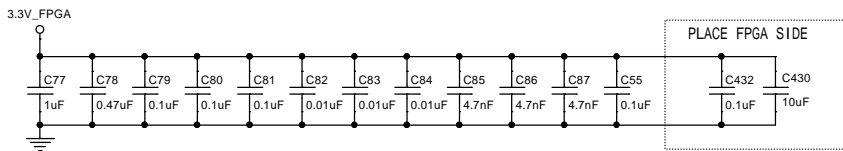
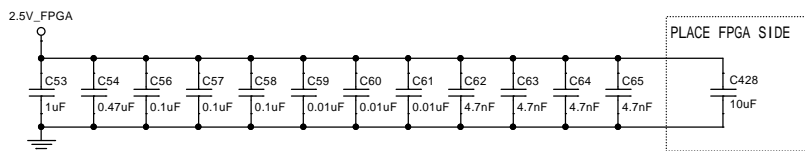
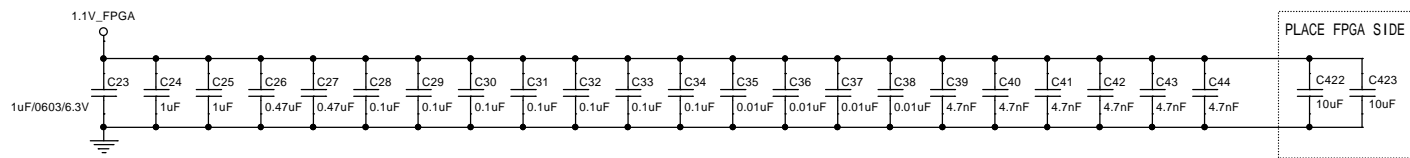
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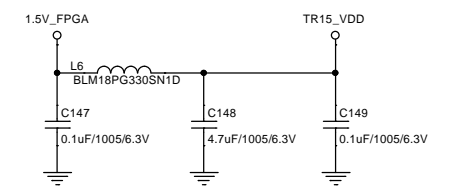
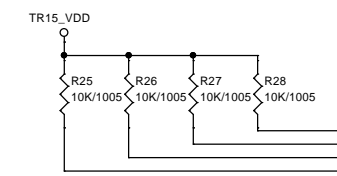
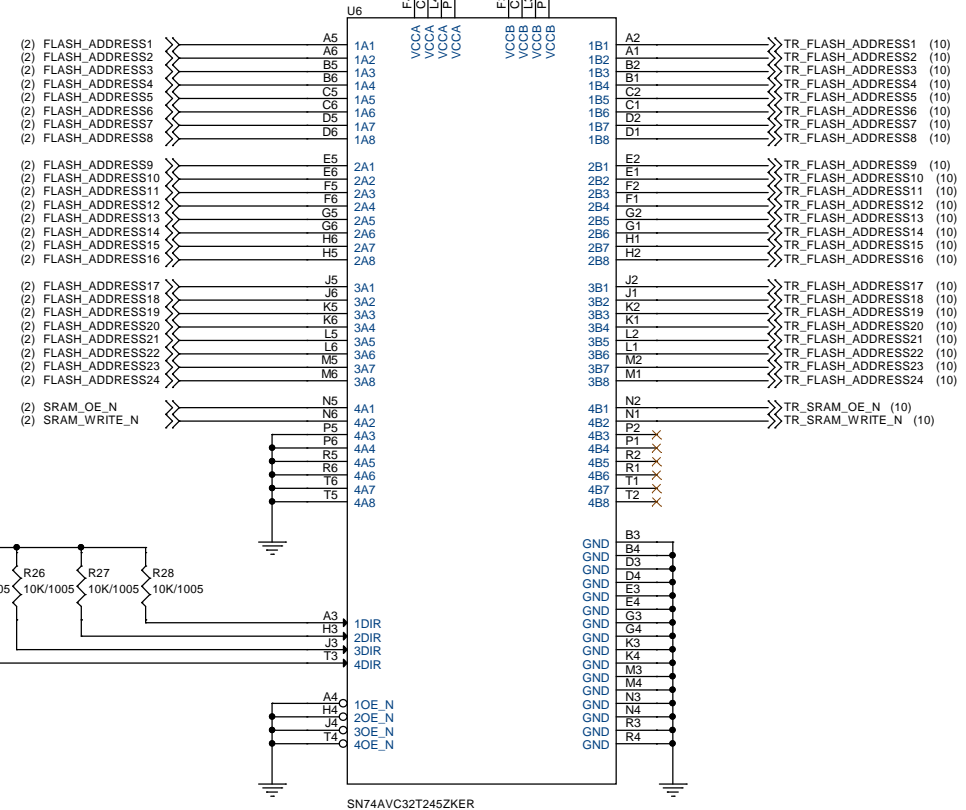
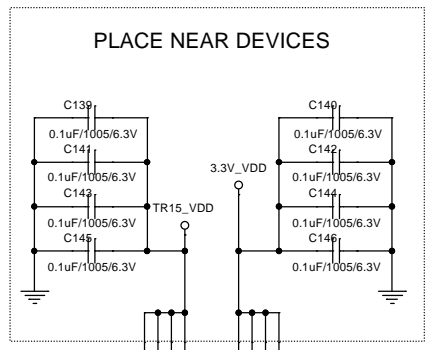
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PLACE NEAR FPGA DEVICES

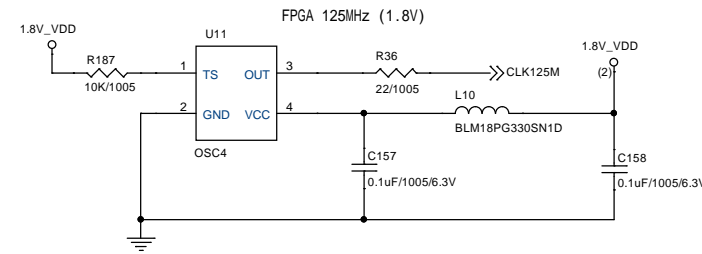
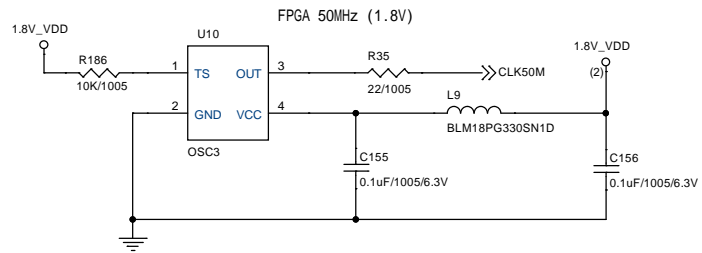
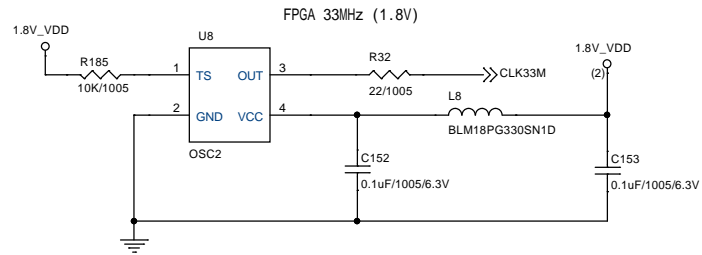
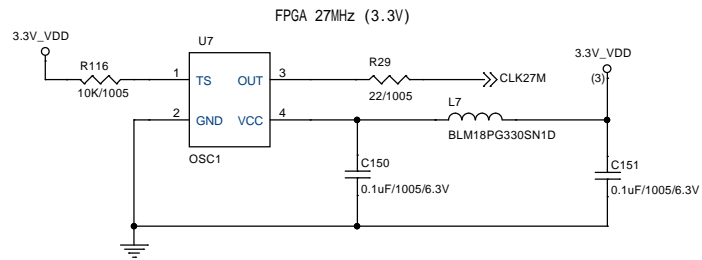
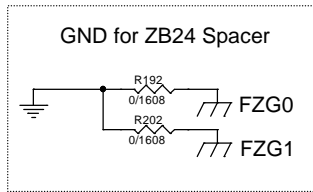
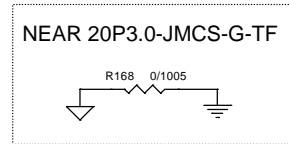
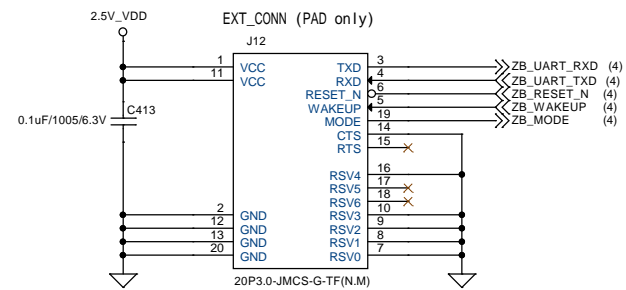
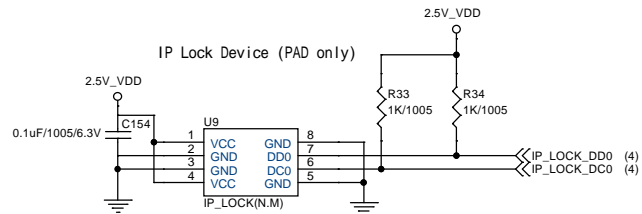
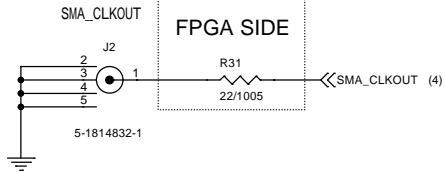
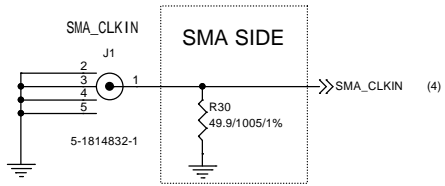


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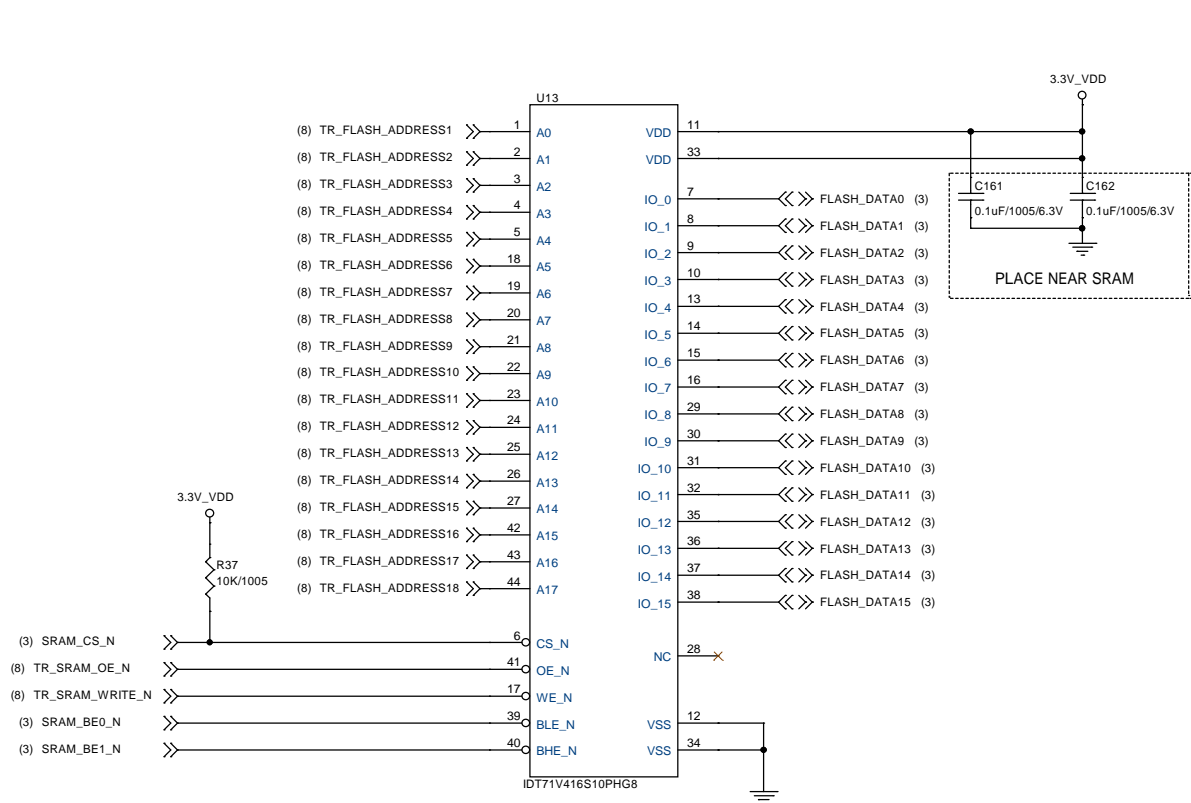
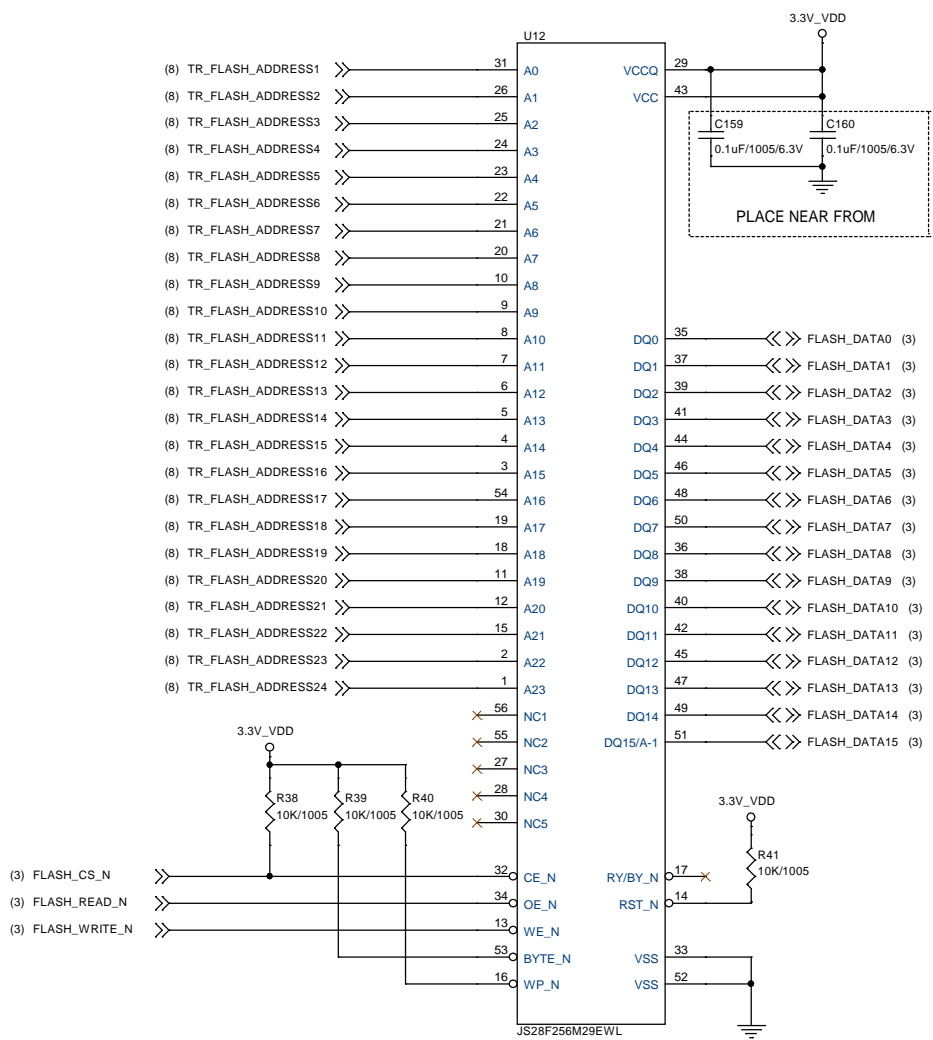


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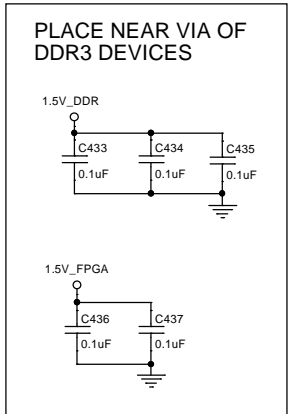
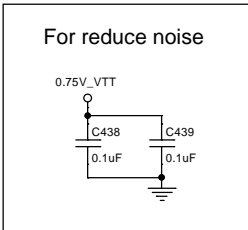
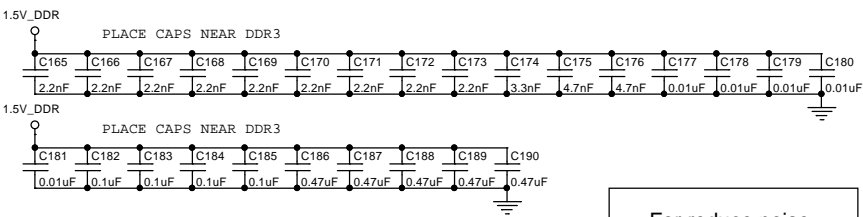
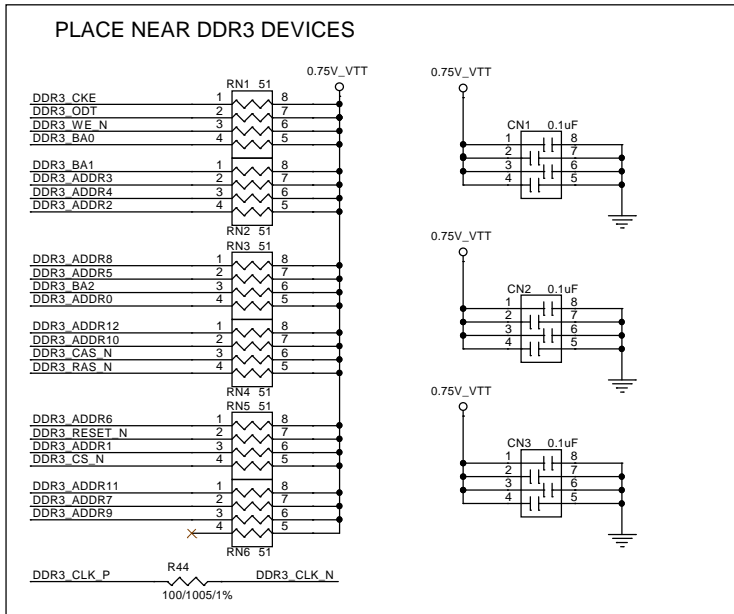
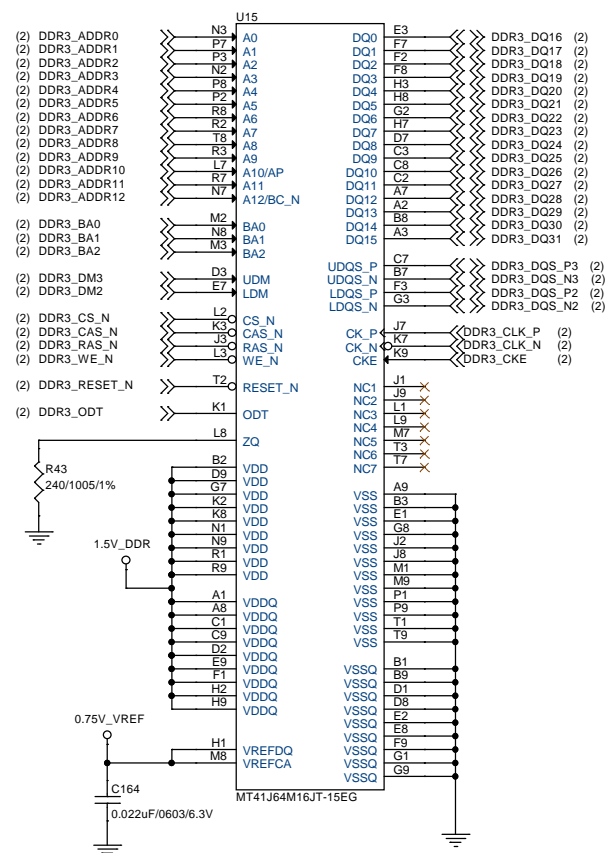
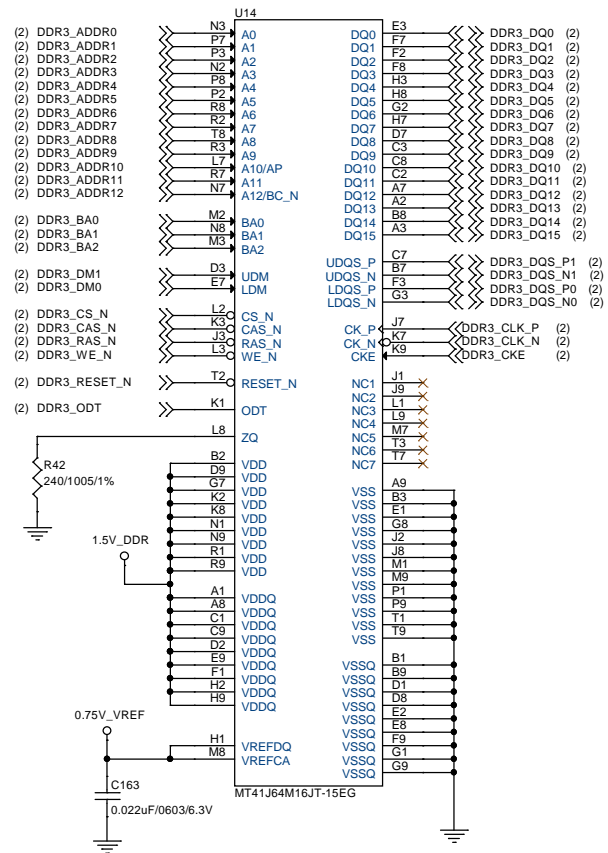




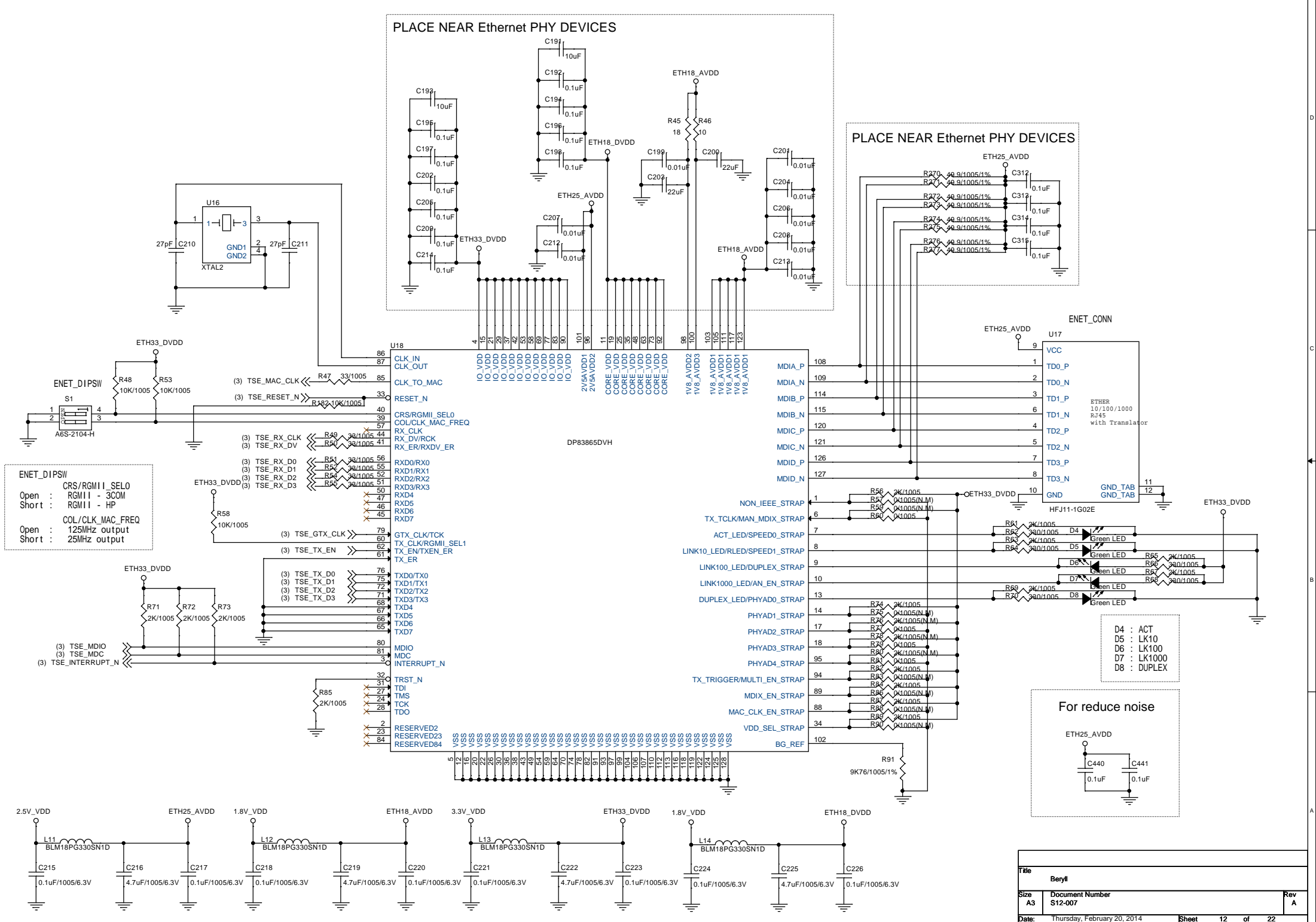
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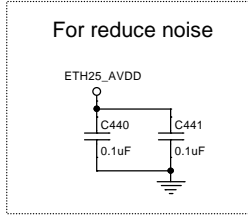
PLACE NEAR Ethernet PHY DEVICES

PLACE NEAR Ethernet PHY DEVICES

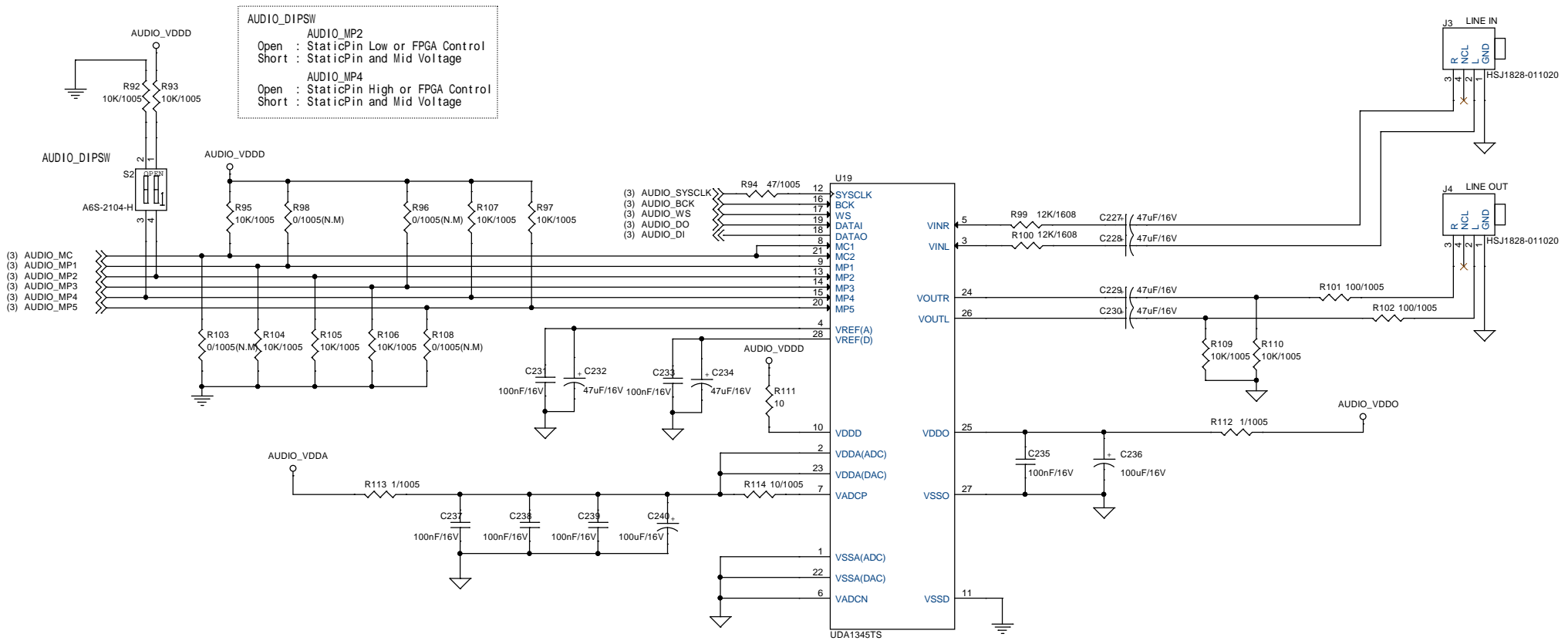
**ENET\_DIPSW**  
 Open : CRS/RGMII\_SELO  
 Short : RGMII - 3COM

**ENET\_DIPSW**  
 Open : COL/CLK\_MAC\_FREQ  
 Short : 125MHz output

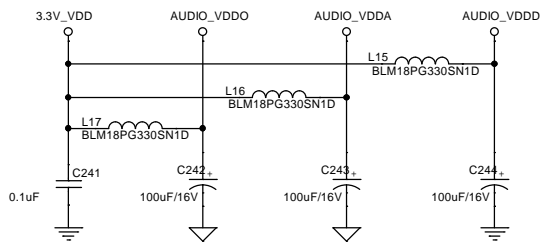
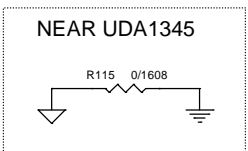
D4 : ACT  
 D5 : LK10  
 D6 : LK100  
 D7 : LK1000  
 D8 : DUPLEX



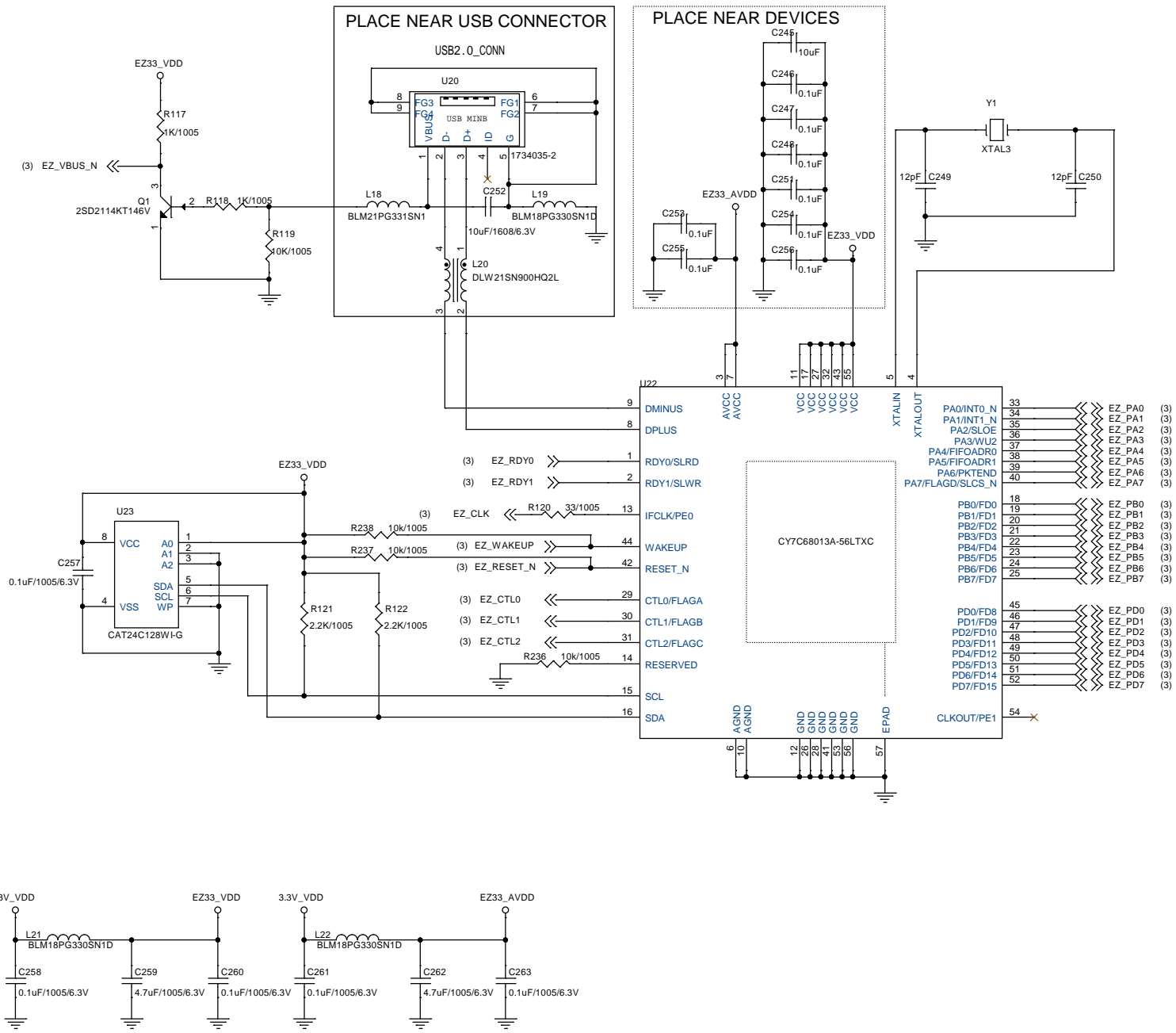
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AUDIO\_DIPSW  
 AUDIO\_MP2  
 Open : StaticPin Low or FPGA Control  
 Short : StaticPin and Mid Voltage  
 AUDIO\_MP4  
 Open : StaticPin High or FPGA Control  
 Short : StaticPin and Mid Voltage

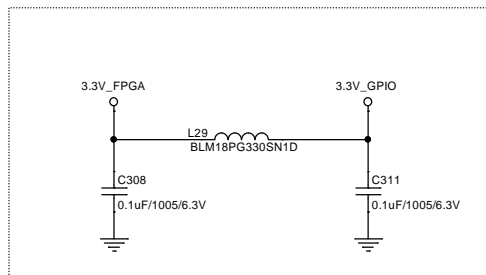
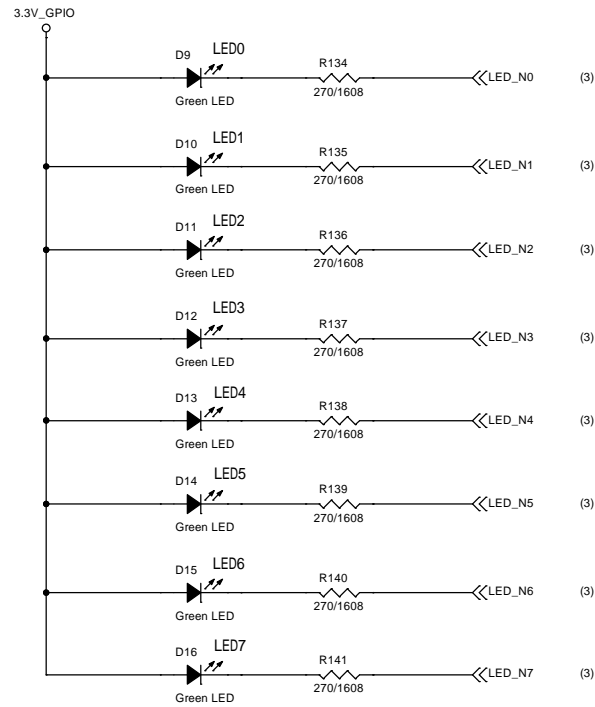
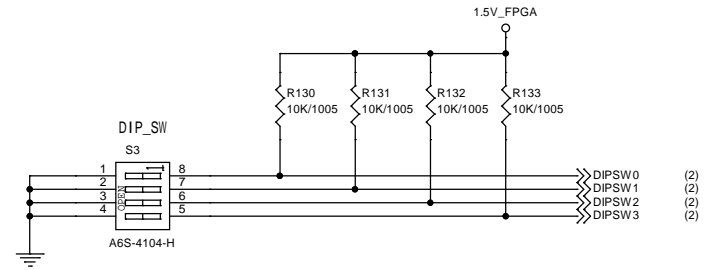
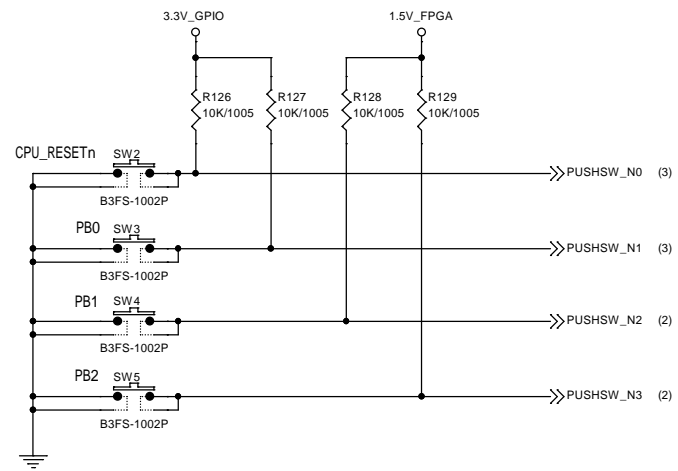


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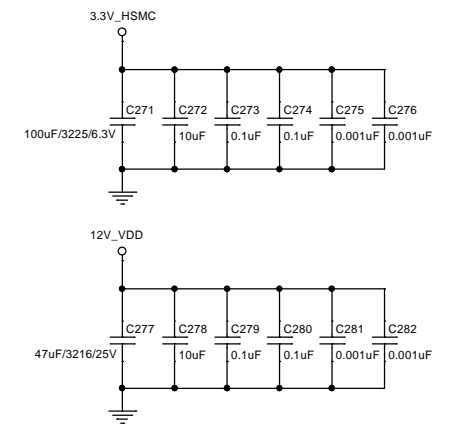
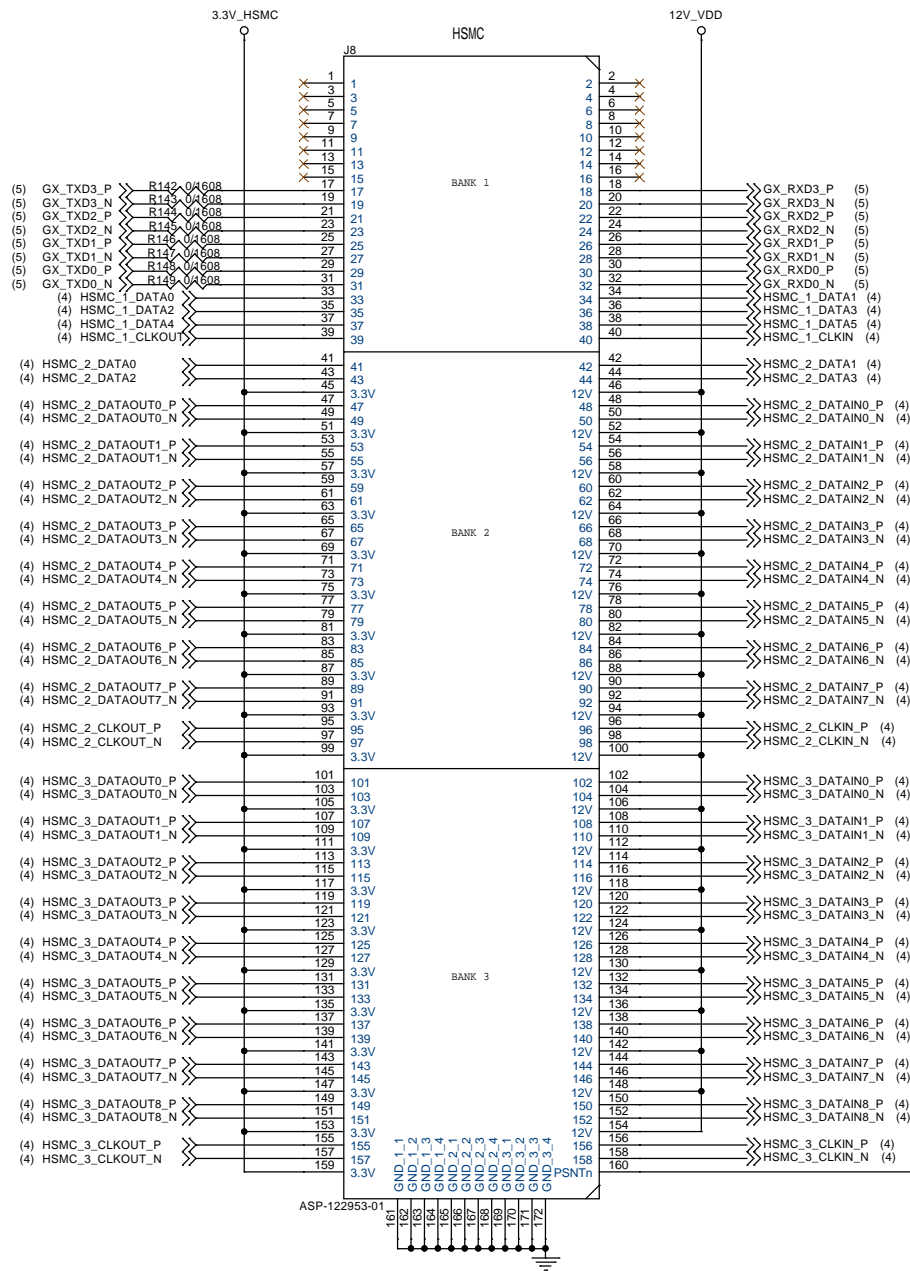
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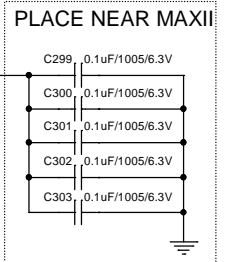
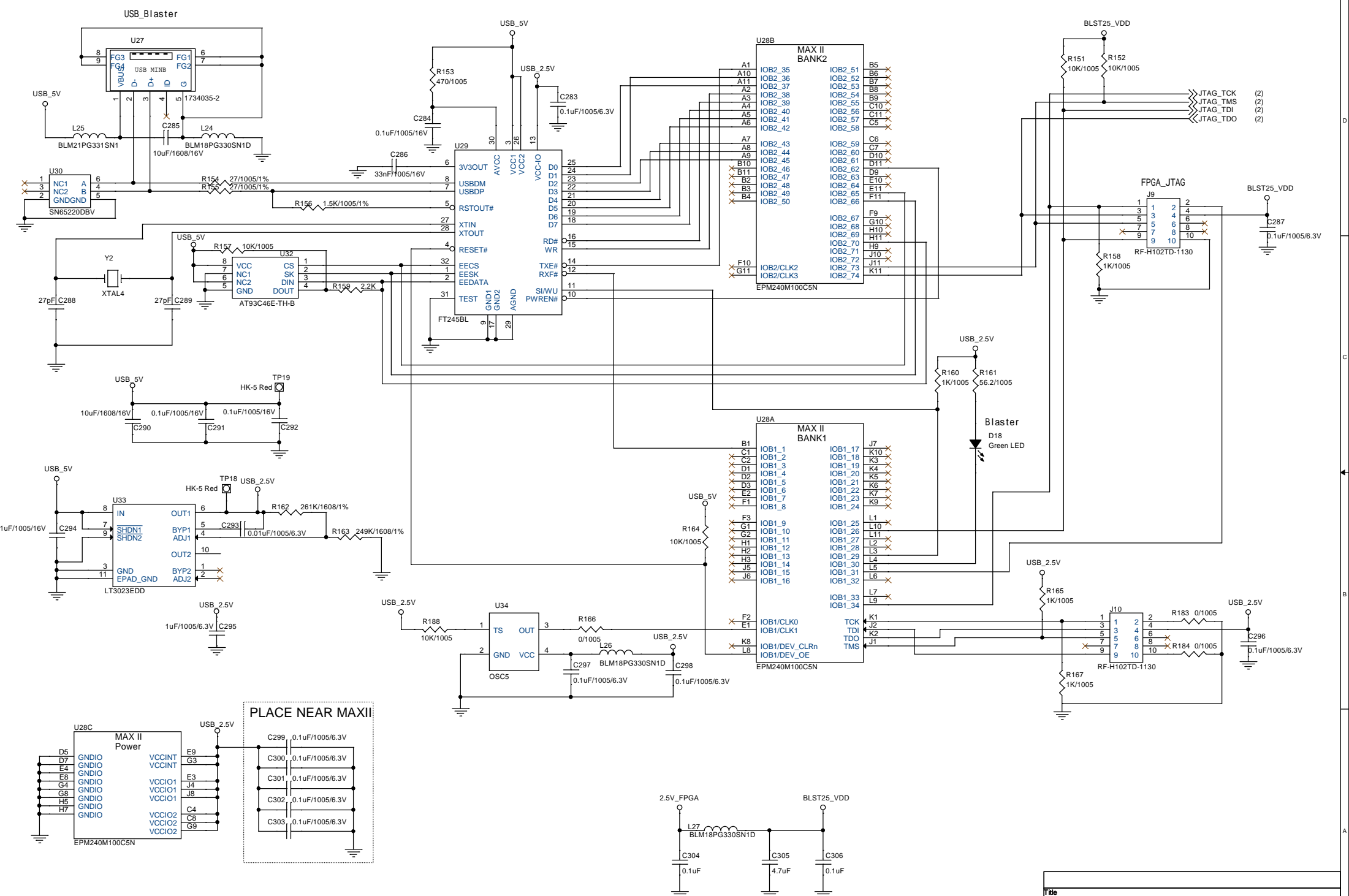


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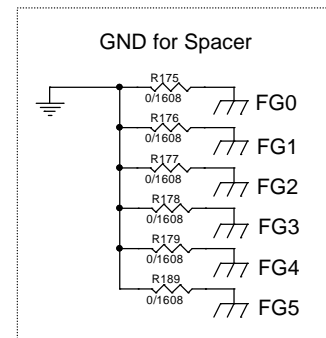
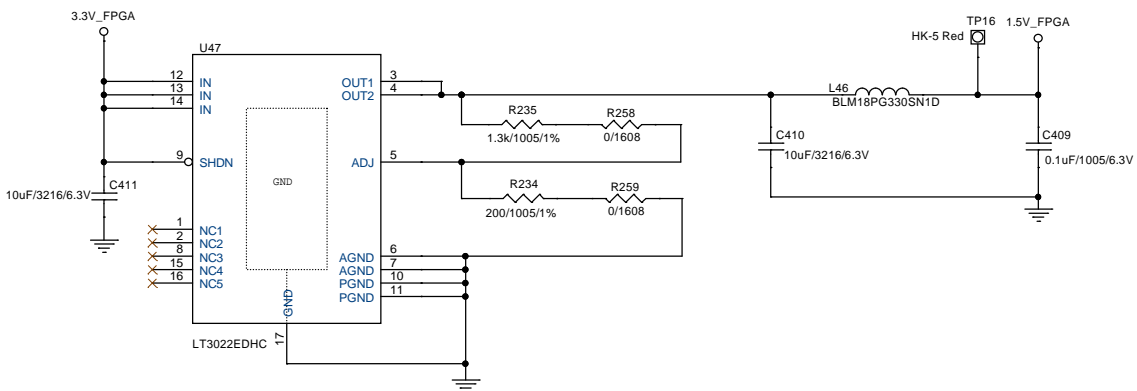
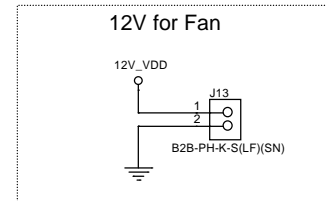
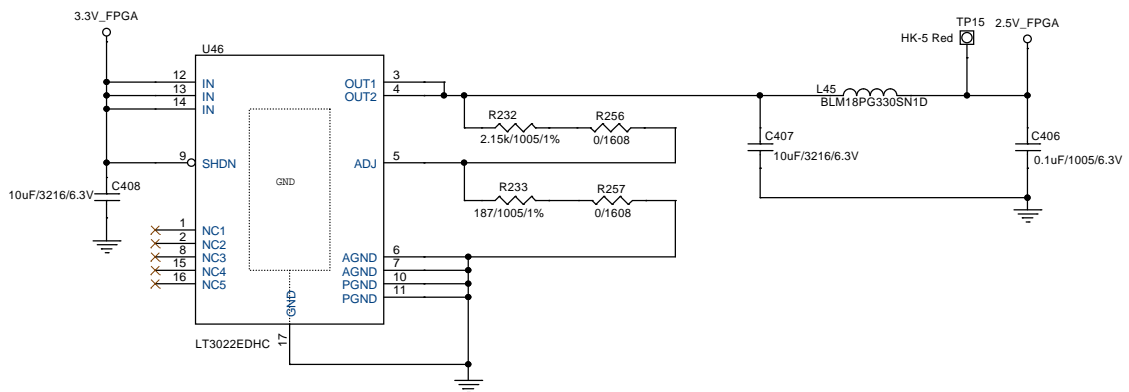
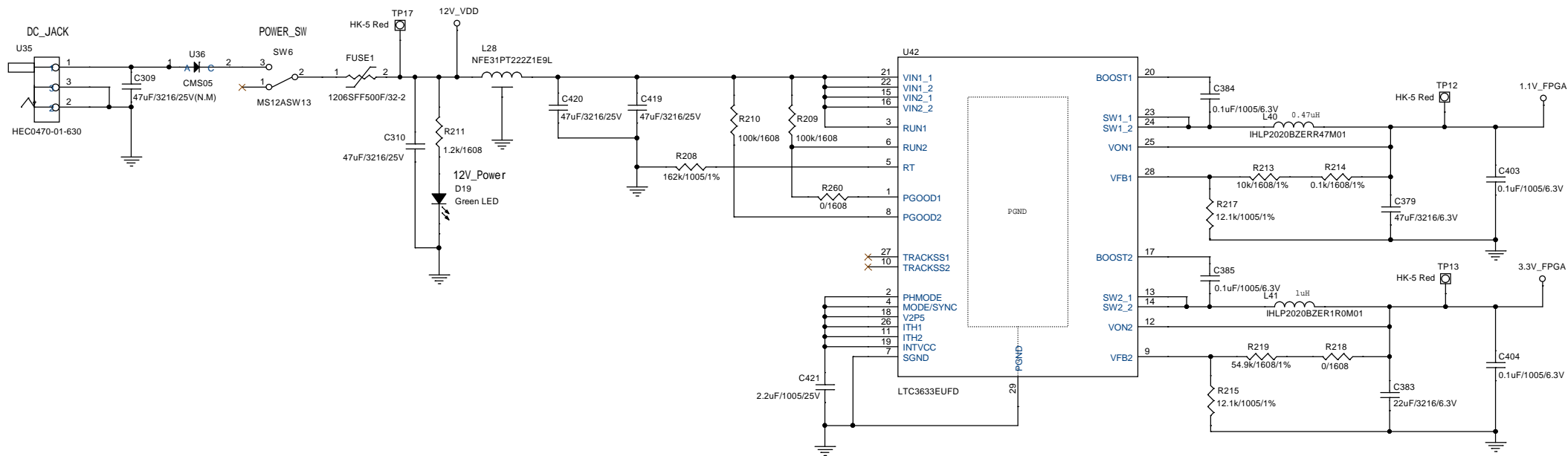




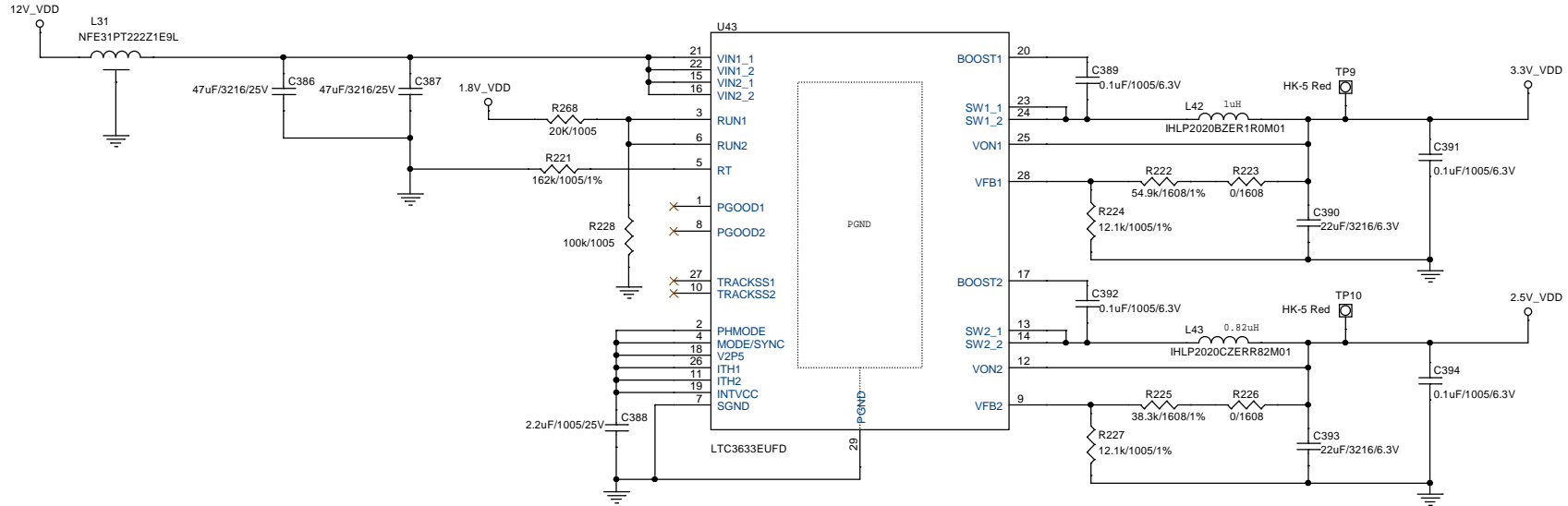
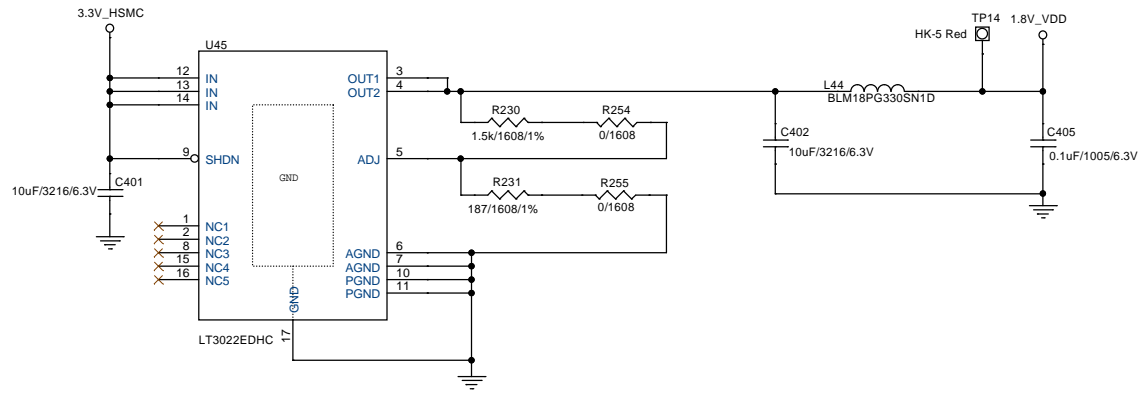
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